cont A9

layer further includes an impurity introduction layer of the same conductivity type as said prescribed conductivity type positioned under said compound layer.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-14 are presently active in this case. Claims 1 and 5 have been amended and claims 11-14 have been added by way of the present amendment.

First, Applicants acknowledge with appreciation the courtesy of an interview granted to Applicants' attorney on August 20, 2002 at which time the subject invention was explained in light of Applicants' disclosure, the outstanding issues were discussed, and arguments substantially as hereinafter developed were presented. No agreement was reached.

In the outstanding Office Action, Figures 22-32 were objected to for not being designated as prior art; Figure 1 was objected to for not including a reference to element 70S; the disclosure was objected to regarding a typo; Claims 1 and 5-9 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,843,813 to Wei et al.; Claims 1 and 10 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,384,455 to Nishigori; and Claims 1-4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,519,243 to Kikuda et al. in view of the Wolfe publication.

In response to the objection to the drawings, submitted herewith is a separate Letter Requesting Approval for Drawing Changes. The drawings will be changed to designate Figures 22-32 as background art. Figures 1, 14, 16, 18, and 21 will be changed in order to identify element 70S. Lastly, Figures 25, 30, and 31 will be changed to identify element 11P. No further objection on this basis is therefore anticipated.

In response to the objection to the disclosure, the specification has been amended to

correct the non-substantive errors on page 2, line 14; page 14, line 15; page 18, line 21; page 19, line 15; page 21, line 10; and page 24, line 18. No new matter has been added. Hence, no further objection on this basis is therefore anticipated.

Briefly recapitulating, the present invention (Claim 1 as amended) provides a semiconductor device including a first well at which a first semiconductor element is provided, a second well at which a semiconductor element is provided, and a first conductive layer which electrically connects the first well and the second well.[1]

Regarding the claim amendments, the phrase "formed by lowering the resistivity of said surface" has been deleted in order to broaden the scope of the invention by removing the requirement of having to check the lowered resistivity in object products. Claim 12 has been added because none of the cited prior art discloses a contact which is obtained in a shallow well. The purpose of adding claim 13 is to distinguish over the prior art documents from a different point of view from claim 1, in view of the fact that recent devices have cobalt silicide formed in a diffusion region.

Wei et al. fail to disclose "a first well at which a first semiconductor element is provided" and "a second well at which a second semiconductor element is provided" as recited in amended claim 1. A semiconductor element is not provided at n-wells 274 and 264 shown in Wei et al.'s Figure 10B. Field oxides 268 and 278 are insulators, not semiconductors. Wei et al. further fail to suggest forming a semiconductor element due to the fact that the n-wells 274 and 264 are part of a resistive source in a single transistor having a gate 252, and there is absolutely no reasonable motivation to form another semiconductor element in the source of the single transistor. Consequently, Wei et al. further fail to suggest forming a semiconductor element due to the fact that the n-wells 274 and 264 are part of a

[1]Amendments to claim 1 are supported by the original disclosure of MOSFETs 91 and 92 and page 6 lines 12-18 and page 14 lines 14-16 of the specification.

resistive source in a single transistor having a gate 252, and there is absolutely no reasonable motivation reason to form another semiconductor element in the source of the single transistor. Consequently, Wei et al. are not believed to anticipate or render obvious the invention of claim 1.

Nishigohri fails to disclose "a first well at which a first semiconductor element is provided" as recited in amended claim 1. While a semiconductor element formed of a transistor having a gate 33 and a diffusion layer 35 is provided at a well 31 in Nishigohri's Figure 16 which the Office action asserts corresponds to the second well of the present invention. A semiconductor element is not provided at region 41 which the Office action asserts corresponds to the first well of the present invention. Moreover, there is no suggestion of forming a semiconductor element. This is due to the fact that region 41 has a different impurity concentration profile from that of well region 31 at which a semiconductor element is provided in order to increase an isolation breakdown voltage between the n-well region 31 and a p-well region 30. The impurity concentration profile not being suitable for forming a semiconductor element. Moreover, there is absolutely no motivation to form a semiconductor element in such a region as 41. Consequently, Nishigohri is not believed to anticipate or render obvious the invention of claim 1.

Kikuda et al. fail to disclose "a first conductive layer electrically connects the first well" as recited in amended claim 1. The wells 4 and 33 in Kikuda et al.'s Figure 3 are electrically separated from each other. Namely, the well 6 which the Office action asserts corresponds to the first conductive layer of the present invention is not electrically connected to the wells 4 and 33. Moreover, there is no suggestion of connecting the wells 4 and 33 by the well 6. This is due to the fact that there is absolutely no reason for connecting the wells 4 and 33 when different voltages V_{CC} and V_R are provided to the wells 4 and 33, respectively. Further, there is absolutely no reasonable motivation either to cause a short circuit between

the power supply voltage V_{CC} (or V_R) and a ground voltage V_{SS} that develops when the well 6 connects the wells 4 and 33. Consequently, Kikuda et al. are not believed to anticipate the subject matter defined by claim 1.

Wolf also fails to disclose "a first conductive layer electrically connects the first well and the second well" as recited in amended claim 1. Accordingly, Kikuda et al. fails to render obvious the subject matter of claim 1 when considered in combination with Wolf.

In light of the above discussion, it is respectfully submitted that Claim 1 is patentably distinguishable from the applied patents and publication, and the dependent Claims 2-12 are therefore also patentably distinguishable from the applied patents and publication.

Regarding newly added claims 13 and 14, the recited feature that "a conductive layer includes a compound layer of the material for the semiconductor substrate and a metal" is not disclosed in Wei et al., Nishigohri, Kikuda et al., or Wolf. Accordingly, the combination of these prior art documents would not teach or suggest the same. Hence, claims 13 and 14 are also believed to be in condition for allowance.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

W. Todd Baker

Gregory J. Maier
Registration No. 25,599
Attorney of Record
W. Todd Baker
Registration No. 45,265

22850
(703) 413-3000
(703) 413-2220 (fax)
GJM:WTB/bwt:jmr
I:\atty\Wtb\2524\201540US\201540us-am.wpd

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Serial No: 09/754,325
Amendment Filed on: HEREWITH
10-25-02

IN THE SPECIFICATION

Please replace the paragraph on page 2, beginning on line 6 as follows:

An NMOSFET 91P is formed on the P well 11P, and a P-type semiconductor layer (hereinafter also referred to as "P-type layer") 21P for fixing the potential of the P well 11P is formed in the P well 11P. Similarly, an NMOSFET 92P different in characteristic from the aforementioned NMOSFET 91P is formed on the P well 12P, and a P-type layer 22P for fixing the potential of the P well 12P is formed in the P well 12P. While the P-type layers 21P and 22P are formed in the vicinity of the boundary between the P wells 11P and 12P in Fig. 22, the P-type layers 21P and 22P may alternatively be formed on other portions in the P wells 11P and 12P respectively. Element isolation films 51P and [51B] 51BP isolate the NMOSFETs 91P and 92P and the P-type layers 21P and 22P from each other.

Please replace the paragraph on page 14, beginning on line 9 as follows:

In particular, the semiconductor device 1 has the area AR3 extending over the adjacent areas AR1 and AR2 with the minimum distance. The area AR3 includes areas overlapping with the areas AR1 and AR2 respectively, and the P wells 11 and 12 are partially arranged in the area AR3. A conductive layer (or first conductive layer) 20 is formed in the surface 50S located in the area AR3 (to extend) over the P wells 11 and 12. In more detail, the conductive layer 20, having an end provided on the P well 11 and another end provided on

the P well [p12]12, electrically connects the P wells 11 and 12 with each other.

Please replace the paragraph on page 18 beginning on line 20 as follows:

In addition to or in place of the NMOSfets 91 and 92, memory cells of a DRAM (dynamic random access memory) or an EEPROM (electrically erasable and programmable read only memory) may be formed in the areas AR1 and AR2. In this case, a step of forming memory capacitors is added. A plurality of wiring layers are formed at need for completing an LSI.

Please replace the paragraph on page 19, beginning on line 13 as follows:

Further, according to the semiconductor device 1, P-type layers 21P and 22P and contacts 31P and 32P may not be provided for P wells 11P and 12P dissimilarly to the conventional semiconductor [layer] device 1P (see Fig. 22). In addition, the P-type layer 20 is provided in the area AR3 to connect the adjacent P wells 11 and 12 with the minimum distance without providing the conventional element isolation film 51BP. Therefore, the layout area for the P-type layer 20, the contacts 31 and 32 and the wire 40 can be reduced as compared with the conventional semiconductor device 1P. Thus, the overall size of the semiconductor device (or chip) 1 can be reduced. Consequently, the number of semiconductor devices obtainable from a unit wafer is increased so that the cost can be reduced.

Please replace the paragraph on page 21, beginning on line 9 as follows:

Only a contact 32 may be provided in place of the contact 31. In this case, the contact [31] 32 corresponds to "first contact", the P well 12 corresponds to "first well" and the P well 11 corresponds to "second well".

Please replace the paragraph on page 24, beginning on line 4 as follows:

While the silicon layer 20a is entirely formed deeper than the silicide layer 20b from the surface 50S here, the silicon layer 20a may be formed to enclose the silicide layer 20b in the surface 50S, i.e., the silicide layer 20b may be formed in the silicon layer 20a. In the semiconductor device 4, a contact 33 is arranged in contact with the silicide layer [21b] 20b of the conductive layer 21B.

IN THE CLAIMS

Please amend Claims 1 and 5 as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first well of a prescribed conductivity type at which a first semiconductor element is provided, said first well being selectively formed in a surface of said semiconductor substrate;

a second well of the same conductivity type as said prescribed conductivity type at which a second semiconductor element is provided, said second well being selectively formed in said surface of said semiconductor substrate;

a first conductive layer across said first well and said second well in said surface of said semiconductor substrate with an end provided on said first well and another end provided on said second well, [formed by lowering the resistivity of said surface] said first conductive layer electrically connecting said first well and said second well; and

a first contact electrically connected with said first well.

5. (Amended) A semiconductor device according to claim 1, further comprising:

a second conductive layer formed in said surface of said semiconductor substrate [by lowering the resistivity of said surface] and provided on said first well without being in

contact with said second well, wherein

said first contact is in contact with said second conductive layer.

11. (New)

12. (New)

13. (New)

14. (New)